REMARKS

Applicants respectfully request reconsideration of this application in view of the foregoing amendments and the following remarks.

Claim Status

Claims 1-17 are pending in this application. Claims 1-17 have been rejected. Claims 8, 10 and 11 are herein amended. No new matter has been added by these amendments.

Objections to the Drawings

The Examiner has objected to FIG. 1 because "the HV line output from element 210 appears to be [mislabeled] as 'Write Buffer'". Applicants have amended FIG. 1 by removing the term "Write Buffer" from its location near the HV line.

The Examiner objected to FIGS. 1, 4 and 5 because "the meaning of the dotted portion of element 180 (write buffer) is unclear". Applicants have amended FIGS. 1, 4 and 5 by removing the dotted portion near the Write Buffer.

The Examiner further objected to FIGS. 1, 4 and 5 because "the interconnection between element 220 (data register) and element 180 (write buffer) is shown as a multiple line interconnection ... [yet the specification] recites 'serially transferring a group of data bits to the nonvolatile memory'". Thus, according to the Examiner, "[t]his serial transfer of data would imply a single line interconnection as opposed to the multiple lines illustrated". Applicants have amended FIGS. 1, 4 and 5 to show a single line connection between the Data Register and the Write Buffer.

Based on the above amendments, reconsideration of the objections to the drawings is respectfully requested.

Objections t the Specification

The Examiner objected to the specification because of two informalities. In particular, the Examiner indicated that "on page 9, line 21 and on page 11, line 11, reference is made to a time value of 30 seconds which appears to be inconsistent with the [specification]". Applicants have amended the specification to indicate a time value of 30μs. Reconsideration of the objections is respectfully requested.

Rejections Under 35 U.S.C. § 112

Claims 1-17 have been rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. In particular, the Examiner asserted "the mechanism or steps by which data is transferred from the controller to the nonvolatile memory is unclear" and "that there appears to be a discrepancy ... as to whether this is a serial or a parallel transfer". The amendments to FIGS. 1, 4 and 5 illustrating the serial transfer of data from the controller to the nonvolatile memory are believed to clarify the discrepancy. As such, reconsideration of this rejection is respectfully requested.

Claims 2, 8, 10-12 and 15 have also been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Specifically, the Examiner indicated that the recitation in claims 2, 8, 12 and 15 "determining the capacity of the nonvolatile memory" be clarified because the "specification appears to utilize the determination of the write data bus width or the write buffer size ... [instead of] the capacity of the entire nonvolatile memory". Applicants respectfully disagree.

Applicants direct the Examiner to page 8, line 21-page 9, line 4, page 8, lines 19-20 and page 10, line 21-page 11, line 10 to further elucidate the claim limitation

"determining the capacity of the nonvolatile memory". As indicated, for example, on page 8, line 21-page 9, line 4, "the command register 250 is programmed [with] data informing a write data bus width (or write buffer size) of the nonvolatile memory chip 100". A byte select register 240 is then used to output a select signal "indicating a write data bus width to the control logic 210 according to the programmed value of the command register 250". Then, "[t]he control logic 210 recognizes the write buffer capacity of the nonvolatile memory chip 100 ..."

In other words, the command register 250 is programmed with data associated with the capacity of the nonvolatile memory chip 100 which could be a write data bus width or write buffer size. Once the command register 250 is programmed with the capacity data the capacity of the nonvolatile memory chip 100 is determined by the control logic 210 upon receiving the select signal from the byte select register 240, which as mentioned above, "[indicates] a write data bus width [or a write buffer size] to the control logic 210 according to the programmed value of the command register 250". As such, Applicants believe claims 2, 8, 12 and 15 as presently written are not indefinite. Reconsideration of this rejection is respectfully requested.

Claim 8 was further rejected as it recites "while transferring a next group of data bits to the nonvolatile memory", which according to the Examiner, are "transferred to the controller while programming the nonvolatile memory". Claim 8 has been amended to recite "a controller for ... enabling the programming of the group of data bits in the nonvolatile memory while ~~transferring~~ a next group of data bits is transferred to the ~~nonvolatile memory~~ controller." Reconsideration of this rejection is respectfully requested.

Claim 10 was rejected as it recites an "embodied voltage generator" which the Examiner indicated as being unclear. Claim 10 has been amended to recite "... the memory chip further [comprising] ~~an embodied~~ voltage generator ..." As such, reconsideration of this rejection is respectfully requested.

Claim 11 was rejected as it recites "performing of the stored data bits" which the Examiner indicated as being unclear. Claim 11 has been amended to recite "... a control logic for ... enabling a program enable signal for the programming ~~performing~~ of the stored data bits in the nonvolatile memory". Reconsideration of this rejection is also respectfully requested.

Rejections Under 35 U.S.C. § 103

Claims 1, 3-6 and 8-17 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,483,748 (Futatsuya) in view of U.S. Patent No. 5,432,741 (Devore) and further in view of U.S. Patent No. 5,790,572 (Oguro).

Claim 1 of the present invention recites,

> A method for programming a nonvolatile memory by a control system having a controller for controlling transfer of data to be programmed, the method comprising the steps of:
>
> sequentially transferring and storing serial address bits from the exterior to the controller;
>
> sequentially transferring and storing a first group of serial data bits from the exterior to the controller;
>
> determining whether all the serial data bits of the first group are transferred to the controller;
>
> transferring the first group of serial data bits to the nonvolatile memory when all the serial data bits of the first group are transferred to the controller; and
>
> sequentially transferring and storing a second group of serial data bits to the controller, while programming the first group of serial data bits in the nonvolatile memory at the address indicated by the address bits.

As correctly pointed out by the Examiner, Futatsuya does not disclose the method steps (in claim 1) of: determining whether all the serial data bits of the first group are transferred to the controller; and sequentially transferring and storing a second group of serial data bits to the controller, while programming the first group of serial data bits in the nonvolatile memory at the address indicated by the address bits. The Examiner, however, indicated that Futatsuya could be utilized by one of ordinary skill in the art to "simultaneously program a first set of data ... while storing a second set of data in the controller ... thereby providing overall reduction in transfer time". Applicants respectfully disagree.

Futatsuya discloses a nonvolatile semiconductor memory device capable of operating in a background operation mode in which data is externally read out during an erasure/programming operation. In particular, Futatsuya discloses a nonvolatile memory device that includes a control circuit for performing a programming operation based on write data latched in a write data buffer. When programming, data latched in the write data buffer is supplied to a write circuit of a write circuit and internal verify sense amplifier and is then programmed to a selected memory bank. After the data is programmed, the control circuit then reads the data on a memory cell on which programming has been performed to determine whether the programmed memory cell reached a required threshold voltage. This is accomplished by activating an internal sense amplifier, which reads out memory cell data that has been programmed to an erasure/programming verification circuit to determine whether the read out data coincides with the data that is latched in the write circuit. If the programming is insufficient, the internal control circuit again applies a necessary voltage to the memory cells.

As mentioned above, the device of Futatsuya does not disclose or suggest "sequentially transferring and storing a second group of serial data bits to the controller, while programming the first group of serial data bits in the nonvolatile memory ..." as recited in claim 1. Moreover, one of ordinary skill in the art would not look to Futatsuya to make the invention as recited in claim 1 because data, which is initially latched in the write data buffer, remains latched in the write data buffer until a programming operation is complete, thus precluding a new set of data from being latched in the write data buffer while programming. As such, Applicants believe that the invention as recited in claim 1 is patentable over the cited art of record because neither Futatsuya taken alone or in combination with the prior art of record or in view of what would have been obvious to one of ordinary skill in the art, teaches, discloses or suggests the invention as recited therein.

Claim 2 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Futatsuya in view of Devore and further in view of Oguro and in further view of U.S. Patent No. 5,761,732 (Shaberman) and in view of what was obvious to one of ordinary skill in the art.

Although Applicants believe claim 2 to be allowable for at least the reasons discussed above with respect to claim 1 from which it depends. Applicants further believe that the combination of Futatsuya in view of Devore and further in view of Oguro and in further view of Shaberman and in view of what was obvious to one of ordinary skill in the art, does not teach, disclose or suggest the invention as recited therein.

Claim 2 of the present invention recites,

> The method of claim 1 further comprising, before the step of transferring the serial address bits to the controller, the steps of:
>
> determining the capacity of the nonvolatile memory; and
>
> setting an enable period of the programming in the nonvolatile memory according to the result of the step of determining the capacity of the nonvolatile memory.

Shaberman is directed to a method and apparatus for interfacing a memory card with a system having a smaller bus width while maintaining its interchangeability with other systems having larger bus widths. Shaberman discloses, inter alia, using a data bus width indicator signal to indicate whether a data bus between a memory card and a host is 8 bits wide or 16 bits wide. The data bus width indicator is not used by Shaberman to set an enable period for programming a nonvolatile memory as recited in claim 2 of the present invention. Moreover, data access in Shaberman is performed in parallel rather than in a serial fashion like that of the present invention. Accordingly, one of ordinary skill in the art would not look to Shaberman and combine it with the teachings of the prior art of record to make the present invention as recited in claim 2. As such, claim 2 is believed to be allowable.

Claim 7 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Futatsuya in view of Devore and further in view of Oguro and in further view of U.S. Patent No. 6,009,496 (Tsai). Claim 7 is believed to be allowable for at least the reasons discussed above with respect to claim 1 from which it depends.

Claim 8 has been rejected by the Examiner "as being essentially a control system analogous to the method rejected in claim 2". In rejecting claim 8 the Examiner further indicated that "Futatsuya shows a memory chip having a nonvolatile memory for storing data bits and programming stored data bits". Thus, according to the Examiner, it would

have been obvious to one or ordinary skill in the art "to serially transfer a group of data bits to the nonvolatile memory based on the capacity of the nonvolatile memory as this would permit efficient and flexible transfer of data dependent upon the variable enable period as described in the rejection of claim 2". Applicants respectfully disagree.

Claim 8, which was amended for §112 purposes, recites,

> A control system comprising:
> a memory chip having a nonvolatile memory for storing data bits and programming the stored data bits; and
> a controller for determining the capacity of the nonvolatile memory, serially transferring a group of data bits to the nonvolatile memory based on the capacity of the nonvolatile memory, and enabling the programming of the group of data bits in the nonvolatile memory while ~~transferring~~ a next group of data bits <u>is transferred</u> to the ~~nonvolatile memory~~ <u>controller</u>.

In contrast to the present invention recited in claim 8, Futatsuya does not disclose or suggest a controller for enabling the programming of the group of data bits in the nonvolatile memory while a next group of data bits is transferred to the controller. Instead, Futatsuya discloses initially latching data in a write data buffer and keeping it latched in the write buffer until a programming operation is complete thereby precluding a new set of data from being latched in the write data buffer while programming. Thus, one of ordinary skill in the art would not look to Futatsuya and combine it with the prior art of record to make the invention as recited in claim 8. As such, Applicants believe that the invention as recited in claim 8 is patentable because neither Futatsuya taken alone or in combination with the prior art of record or in view of what would have been obvious to one of ordinary skill in the art, teaches, discloses or suggests the invention as recited in claim 8.

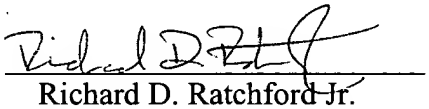
Dependent Claims

Applicants have not independently addressed the rejections of the dependent claims (i.e., 3-6 and 9-17) because Applicants submit that, in view of the amendments to the claims presented herein and, for at least similar reasons as why the independent claims from which the dependent claims depend are believed allowable as discussed, supra, the dependent claims are also allowable. Applicants however, reserve the right to address any individual rejections of the dependent claims should such be necessary or appropriate.

CONCLUSION

Accordingly, Applicants submit that the claims as herein presented are allowable over the prior art of record, taken alone or in combination, and that the respective rejections be withdrawn. Applicants further submit that the application is hereby placed in condition for allowance which action is earnestly solicited.

Respectfully submitted,

By: 

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